IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	Confirmation No.: 7760
Burns *et al.*	Art Unit: 2816
Patent. No.: 7,190,219 B2	Examiner: Tra, Anh Quan
Issued: March 13, 2007	Atty. Docket: 1875.109000A
For: **Extended Range Variable-Gain Amplifier**	

Request for Certificate of Correction Under 37 C.F.R. § 1.322 and 1.323

Attn: Certificate of Correction Branch

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that a Certificate of Correction under 37 C.F.R. §§ 1.322 and 1.323 be issued for the above-captioned United States Patent. This Certificate of Correction is being requested due to mistakes which appear in the printed patent. These mistakes were made by both the U.S. Patent and Trademark Office and by Applicants.

The mistakes made by Applicants are of a clerical or typographical nature, or of a minor character. Patentees submit that correction of these errors does not introduce new matter.

Specifically, the printed patent contains the following errors for which a Certificate of Correction is respectfully requested:

On the cover page, in section (63) of Related U.S. Application Data, "Jul 30, 2001" should be replaced with --Jul. 3, 2001--. The correct filing date of priority appl. No. 09/897,601 is July 3, 2001, as noted in the Application Data Sheet, filed January 20, 2004.

In Figure 1, the reference number "120" that is tagged to the Up-Stream Channels should be replaced with --119--. This error is to correct an inadvertent duplication of the use of reference number 120 in the application. As can be seen in Figure 1, reference number 120 is already used for the High-Pass Filter (labeled "HPF"), which is just above and to the right of the Up-Stream Channels. To correct this duplication, the Up-Stream Channels should be labeled as 119.

Similar to the afore-mentioned Figure correction, at column 2, line 54, "up-stream channels 118" should be replaced with --up-stream channels 119--. In this part of the specification, the up-stream channels were mislabeled with number 118, which is already used by the Low-Pass Filter.

At column 3, lines 48-58 should deleted and replaced with the correct corresponding paragraph **[0024]**, which is reproduced here for convenience:

--Looking now to FIG. 3A, automatic gain control logic decoder 204 is illustrated as comprising automatic gain control amplifiers 350 and a logic circuit array 352. Automatic gain control amplifiers 350 accept automatic gain control voltage 114 and output a plurality of comparator outputs 312(n) which are routed to logic circuit array 352. Logic circuit array 352 outputs the plurality of amplifier control signals. As illustrated in FIG. 3B, automatic gain control amplifiers 350 are preferably comprised of a resistor ladder 302 and thirty-five high-gain, low frequency amplifiers 306.1 through 306.35, and logic circuit array 352 is preferably comprised of thirty-five logic circuits 308.1 through 308.35. Resistor ladder 302 is comprised of a top resistor 303, thirty-four resistors designated as resistors 304.1 through 304.34, and a bottom resistor 305. Top resistor 303 is connected on a first side to a bias potential V_{DD} and on a second side to a

first side of resistor 304.1. The connection point between top resistor 303 and resistor 304.1 is node 301.1. A second side of resistor 304.1 is connected to a first side of resistor 304.2 at a node 301.2. Thus it can be said that for any sequential pair of resistors 304(i) and 304(i+1) in resistor ladder 302, a second side of resistor 304(i) is connected to a first side of resistor 304(i+1) at node 301 (i+1). At the "bottom" of resistor ladder 302, a second side of resistor 304.34 is preferably connected to a first side of bottom resistor 305 at node 301.35, and a second side of bottom resistor 305 is preferably connected to a ground 309. Those skilled in the relevant art(s) will understand, based on the teachings contained herein, that the second side of bottom resistor 305 could be connected to a potential other than ground without deviating from the spirit and intent of the invention. Further, the invention also covers the embodiment wherein the first side of resistor 304.1 is connected directly to bias potential V_{DD} 307, and the second side of resistor 304.34 is connected directly to ground 309.--

On August 9, 2006, Applicants filed an Amendment in which an attempt was made to correct the mislabeling of up-stream channels 118 (which is noted above). However, Applicants inadvertently inserted the incorrect replacement paragraph number into the Amendment. The paragraph that should have been replaced was paragraph **[0020]**, but Applicants inadvertently listed the paragraph number of **[0024]** in the Amendment. Therefore, the patent issued with incorrect text at column 3, lines 48-58.

At column 15, line 41, a period should be inserted after "settings)". This will correct a minor grammatical error.

At column 15, line 50, a period should be inserted after "off". This will correct a minor grammatical error.

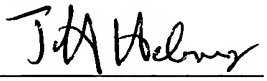
Remarks

The above-noted corrections do not involve such changes in the patent as would constitute new matter or would require reexamination.

A completed Form PTO/SB/44 accompanies this request, with the above-noted corrections printed thereon. Accordingly, a Certificate of Correction is believed proper and issuance thereof is respectfully requested.

This request is accompanied by payment of the fee set forth in 37 C.F.R. § 1.20(a). Fee payment is provided in the attached Credit Card Payment Form (PTO-2038). The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Jeffrey T. Helvey
Agent for Applicants
Registration No. 44,757

Date: 2/8/2008

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: 7,190,219 B2

DATED: March 13, 2007

INVENTORS: Burns *et al.*

It is certified that error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below.

Cover Page
At section (63), under Related U.S. Application Data, "Jul. 30, 2001" should be replaced with --Jul. 3, 2001--.

Drawings
In Figure 1, please replace the up-stream channels reference number "120" with --119--.

Column 2
At line 54, please replace "up-stream channels **118**" with --up-stream channels **119**--.

Column 3
Please delete lines 48-58 and replace with the following paragraph:
-- Looking now to FIG. 3A, automatic gain control logic decoder 204 is illustrated as comprising automatic gain control amplifiers 350 and a logic circuit array 352. Automatic gain control amplifiers 350 accept automatic gain control voltage 114 and output a plurality of comparator outputs 312(n) which are routed to logic circuit array 352. Logic circuit array 352 outputs the plurality of amplifier control signals. As illustrated in FIG. 3B, automatic gain control amplifiers 350 are preferably comprised of a resistor ladder 302 and thirty-five high-gain, low frequency amplifiers 306.1 through 306.35, and logic circuit array 352 is preferably comprised of thirty-five logic circuits 308.1 through 308.35. Resistor ladder 302 is comprised of a top resistor 303, thirty-four resistors designated as resistors 304.1 through 304.34, and a bottom resistor 305. Top resistor 303 is connected on a first side to a bias potential VDD and on a second side to a first side of resistor 304.1. The connection point between top resistor 303 and resistor 304.1 is node 301.1. A second side of resistor 304.1 is connected to a first side of resistor 304.2 at a node 301.2. Thus it can be said that for

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(Continued from page 1)

any sequential pair of resistors 304(i) and 304(i+1) in resistor ladder 302, a second side of resistor 304(i) is connected to a first side of resistor 304(i+1) at node 301 (i+1). At the "bottom" of resistor ladder 302, a second side of resistor 304.34 is preferably connected to a first side of bottom resistor 305 at node 301.35, and a second side of bottom resistor 305 is preferably connected to a ground 309. Those skilled in the relevant art(s) will understand, based on the teachings contained herein, that the second side of bottom resistor 305 could be connected to a potential other than ground without deviating from the spirit and intent of the invention. Further, the invention also covers the embodiment wherein the first side of resistor 304.1 is connected directly to bias potential VDD 307, and the second side of resistor 304.34 is connected directly to ground 309.--

Column 15
At line 41, please insert a period after "settings)".
At line 50, please insert a period after "off".

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